Course Syllabi

CODE 203

NAME Computer Organization

Credits 6 ECTS

Period Fall Semester

Course Specifications
Lectures in the classroom, individual work, questionnaires on-line by virtual campus and laboratory work
Objectives and contents
The objective of the subject is to understand the internal organization of a computer (from a hardware point of view).
Contents:

Theory

Topic 1. Improving Processor Performance with Pipelining (50%)
a. Performance Measurement and Amdahl's Law
b. RISC-V Pipelining
c. Data Hazards
d. Control Hazards
e. Advanced Parallelism

Topic 2. Memory Hierarchy (30%)
a. Introduction
b. Cache Memory
c. Improving Memory System Bandwidth: Interleaving
d. Virtual Memory: Paging

Topic 3. Input/Output and Peripherals (20%)
a. Devices, Controllers, and Input/Output Ports
b. Input/Output Programming:
a. Programmed I/O
b. Interrupt-Driven I/O
c. Direct Memory Access (DMA)

Lab Work

Lab 1. RISC-V Pipelining
Lab 2. Cache
Lab 3. Input/Output
Lab 4. Advanced Code Optimization Techniques

Assessment

There will be no final exam in the first ordinary session, where the continuous assessment method is applied. This continuous assessment will consist of mandatory partial tests (C1, C2, C3) conducted throughout the course, which will cover the theoretical and practical content of the three course topics. There is no minimum required score for each test, except for the final test of the course, which requires a minimum score of 3 (out of 10). Based on the test results, a weighted average grade will be calculated as follows:
average_grade = 0.50**C1* **+** ***0.30******C2 + 0.20*C3**

The exams will be held in laboratories. During the exams, students will not have access to AI tools.

To calculate the final grade, students with an average_grade of 5 or higher may receive up to 1 additional point from activities proposed by the teaching staff throughout the course, with the final grade capped at 10.

Lecturer
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